Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-22 (CANCELLED)

23. (NEW) A lateral power MOSFET semiconductor device comprising:

a. a semiconductor substrate;

b. a plurality of first doped regions in said semiconductor substrate forming a plurality of source elements; said source elements being arranged in one or more rows defined by a layer of silicide;

c. a plurality of second doped regions in said semiconductor substrate forming a plurality of drain elements; said drain elements being arranged in one or more rows defined by a layer of silicide and interleaved with said plurality of source elements rows;

d. a first connectivity layer having a plurality of first runners and a plurality of second runners parallel to each other and orthogonal to said rows of source and drain elements, wherein said plurality of first runners are connected to said plurality of source element rows; said plurality of second runners are connected to said plurality of drain element rows; said plurality of first runners being interleaved with said plurality of second runners;

e. a second connectively layer having a plurality of third runners and a plurality of fourth runners, said third and fourth runners being orthogonal to said first and second runners; wherein said plurality of third runners are multiply connected to said plurality of first runners and said plurality of fourth runners are multiply connected to said plurality of second runners; said plurality of third runners being interleaved with said plurality of fourth runners; and;

f. a third connectively layer having a plurality of first pads multiply connected to said plurality of third runners and a plurality of second pads multiply connected to said plurality of fourth runners; said first and second pads being arranged in a checkerboard pattern to form said lateral power MOSFET semiconductor device;

wherein there are multiple electrical paths to said source and drain elements such that electrical current will flow to each of said source and drain elements along an electrical path having a minimum of resistance

24. (NEW) The lateral power MOSFET semiconductor device as in claim 23 wherein said at least one first pad has at least one first solder bump and said at least one second pad has at least one second solder bump.

25. (NEW) A lateral power MOSFET semiconductor device comprising:

a. a semiconductor substrate;

b. a plurality of first doped regions in said semiconductor substrate forming a plurality of source elements; said source elements being arranged in one or more rows defined by a layer of silicide;

c. a plurality of second doped regions in said semiconductor substrate forming a plurality of drain elements; said drain elements being arranged in one or more rows defined by a layer of silicide and interleaved with said plurality of source elements rows;

d. a first connectivity layer having a plurality of first runners and a plurality of second runners parallel to each other and orthogonal to said rows of source and drain elements, wherein said plurality of first runners are connected to said plurality of source element rows; said plurality of second runners are connected to said plurality of drain element rows; said plurality of first runners being interleaved with said plurality of second runners;

e. a second connectively layer having a plurality of first pads multiply connected to said plurality of second runners and a plurality of second pads multiply connected to said plurality of third runners; said first and second pads being arranged in a checkerboard pattern to form said lateral power MOSFET semiconductor device;

wherein there are multiple electrical paths to said source and drain elements such that electrical current will flow to each of said source and drain elements along an electrical path having a minimum of resistance.

26. (NEW) The lateral power MOSFET semiconductor device as in claim 25 wherein said at least one first pad has at least one first solder bump and said at least one second pad has at least one second solder bump.

27. (NEW) A lateral power MOSFET semiconductor device comprising:

a. a semiconductor substrate;

b. a plurality of first doped regions in said semiconductor substrate forming a plurality of source elements; said source elements being arranged in one or more rows defined by a layer of silicide;

c. a plurality of second doped regions in said semiconductor substrate forming a plurality of drain elements; said drain elements being arranged in one or more rows defined by a layer of silicide and interleaved with said plurality of source elements rows;

d. a first connectivity layer having a plurality of first runners and a plurality of second runners parallel to each other and orthogonal to said rows of source and drain elements, wherein said plurality of first runners are connected to said plurality of source element rows; said plurality of second runners are connected to said plurality of drain element rows; said plurality of first runners being interleaved with said plurality of second runners;

e. a second connectively layer having a plurality of third runners and a plurality of fourth runners, said third and fourth runners being orthogonal to said

first and second runners; wherein said plurality of third runners are multiply connected to said plurality of first runners and said plurality of fourth runners are multiply connected to said plurality of second runners; said plurality of third runners being interleaved with said plurality of fourth runners; and;

f. a third connectively layer having a plurality of first pads multiply connected to said plurality of third runners and a plurality of second pads multiply connected to said plurality of fourth runners; said first and second pads being arranged in a striped pattern to form said lateral power MOSFET semiconductor device;

wherein there are multiple electrical paths to said source and drain elements such that electrical current will flow to each of said source and drain elements along an electrical path having a minimum of resistance.

28. (NEW) The lateral power MOSFET semiconductor device as in claim 27 wherein said at least one first pad has at least one first solder bump and said at least one second pad has at least one second solder bump.

29. (NEW) A lateral power MOSFET semiconductor device comprising:

a. a semiconductor substrate;

b. a plurality of first doped regions in said semiconductor substrate forming a plurality of source elements; said source elements being arranged in one or more rows defined by a layer of silicide;

c. a plurality of second doped regions in said semiconductor substrate forming a plurality of drain elements; said drain elements being arranged in one or more rows defined by a layer of silicide and interleaved with said plurality of source elements rows;

d. a first connectivity layer having a plurality of first runners and a plurality of second runners parallel to each other and orthogonal to said rows of source and drain elements, wherein said plurality of first runners are connected to said plurality of source element rows; said plurality of second runners are connected to said plurality of drain element rows; said plurality of first runners being interleaved with said plurality of second runners;

e. a second connectively layer having a plurality of first pads multiply connected to said plurality of first runners and a plurality of second pads multiply connected to said plurality of second runners; said first and second pads being arranged in a striped pattern to form said lateral power MOSFET semiconductor device;

wherein there are multiple electrical paths to said source and drain elements such that electrical current will flow to each of said source and drain elements along an electrical path having a minimum of resistance.

30. (NEW) The lateral power MOSFET semiconductor device as in claim 29 wherein said at least one first pad has at least one first solder bump and said at least one second pad has at least one second solder bump.